

# TS72461K - 10W CW GaN Broadband RF Switch SP4T

## 1.0 Features

- Low insertion loss: 0.40dB @ 800MHz
- High linear power handling
- No external DC blocking capacitors on RF lines
- 40dBm CW hot switching capable
- Versatile 2.6-5.5V power supply
- Operating frequency: 400MHz to 3.8GHz



**Figure 1 Device Image**  
(16 Pin 3×3×0.8mm QFN Package)

## 2.0 Applications

- Cellular infrastructure
- Small cells
- LTE relays and microcells
- Satellite terminals

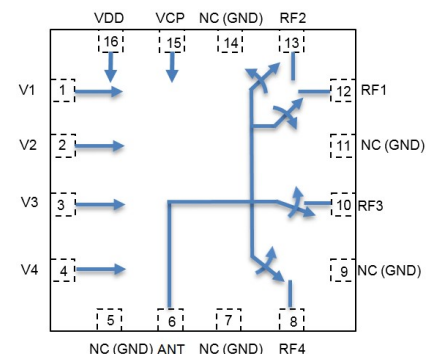


**RoHS/REACH/Halogen Free Compliance**

## 3.0 Description

The TS72461K is a symmetrical reflective Single Pole Four Throws (SP4T) switch based on the cutting edge GaN technology designed for broadband and high power switching applications. Its broadband behavior from 400MHz to 3.8GHz frequencies makes the TS72461K an excellent switch for all applications requiring low insertion loss, high isolation and high linearity within a small package size. The 4 control lines can be selected up to 16 possible positions independently.

The TS72461K is packaged into a compact Quad Flat No lead (QFN) 3x3mm 16 leads plastic package.



**Figure 2 Function block diagram**  
(Top View)

## 4.0 Ordering Information

**Table 1 Ordering Information**

Base Part Number	Package Type	Form	Qty	Reel Diameter	Reel Width	Orderable Part Number
TS72461K	16 Pin 3×3×0.8mm QFN	Tape and Reel	3000	13" (330mm)	18mm	TS72461KMTRPBF
Evaluation Board						TS72461K-EVB

## 5.0 Pin Description

**Table 2 Pin Definition**

Pin Number	Pin Name	Description
1	V1	Switch control input 1
2	V2	Switch control input 2
3	V3	Switch control input 3
4	V4	Switch control input 4
5	NC	No internal connection. Can be grounded
6	ANT	Antenna port
7	NC	No internal connection. Can be grounded
8	RF4	RF port 4
9	NC	No internal connection. Can be grounded
10	RF3	RF port 3
11	NC	No internal connection. Can be grounded
12	RF1	RF port 1
13	RF2	RF port 2
14	NC	No internal connection. Can be grounded
15	VCP	Internal charge pump voltage output. Connect a 1nF capacitor to GND on this pin to improve switching time.
16	VDD	DC Supply voltage

**Note:** The backside ground (thermal) pad of the package must be grounded directly to the ground plane of PCB with multiple vias to ensure proper operation and thermal management.

## 6.0 Absolute Maximum Ratings

**Table 3 Absolute Maximum Ratings @ $T_A=+25^{\circ}\text{C}$  Unless Otherwise Specified**

Parameter	Symbol	Value	Unit
<b>Electrical Ratings</b>			
Power Supply Voltage	VDD	2.6 to 5.5	V
Storage Temperature Range	$T_{st}$	-55 to +125	$^{\circ}\text{C}$
Operating Temperature Range	$T_{op}$	-40 to +85	$^{\circ}\text{C}$
Maximum Junction Temperature	$T_J$	+150	$^{\circ}\text{C}$
RF Input Power CW, 85 $^{\circ}\text{C}$	RFx	41	dBm
Peak RF Power, 1% Duty Cycle, 85 $^{\circ}\text{C}$	RFx	49	dBm
<b>Thermal Ratings</b>			
Thermal Resistance (junction-to-case) – bottom side	$R_{\theta JC}$	$\leq 20$	$^{\circ}\text{C}/\text{W}$
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	$\leq 37$	$^{\circ}\text{C}/\text{W}$
Soldering Temperature	$T_{SOLD}$	$\leq 260$	$^{\circ}\text{C}$
<b>ESD Ratings</b>			
Human Body Model (HBM)	Level 1B	500 to <1000	V
Charged Device Model (CDM)	Level C3	$\geq 1000$	V
<b>Moisture Rating</b>			
Moisture Sensitivity Level	MSL	1	-

### Attention:

Maximum ratings are absolute ratings. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Exceeding one or a combination of the absolute maximum ratings may cause permanent and irreversible damage to the device and/or to surrounding circuit.

## 7.0 Electrical Specifications

**Table 4 Electrical Specifications** @T<sub>A</sub>=+25°C Unless Otherwise Specified; V<sub>DD</sub>=+2.7V; 50Ω Source/Load.

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operating frequency		400		3800	MHz
Insertion loss	800MHz (No Match)		0.40		dB
	1.95GHz (No Match)		0.50		
	2.6GHz (No Match)		0.6	0.8	
	3.8GHz (With Match)		0.90		
Isolation ANT-RFx	800MHz (No Match)		45		dB
	1.95GHz (No Match)		33		
	2.6GHz (No Match)	22	28		
	3.8GHz (With Match)		23		
Return Loss ANT-RFx	800MHz (No Match)		28		dB
	1.95GHz (No Match)		25		
	2.6GHz (No Match)		18		
	3.8GHz (With Match)		15		
H2	800MHz, Pin=35dBm		-42		dBm
H3	800MHz, Pin=35dBm		-45		dBm
IIP3	800MHz		70		dBm
P0.1dB CW <sup>[1]</sup>	800 - 3800MHz, -40°C ~ +85°C	40			dBm
Peak P0.1dB <sup>[1]</sup>	1% duty cycle, 800-3800MHz, -40°C ~ +85°C		48		dBm
Switching time	50% ctrl to 10/90% of the RF value is settled. C1=1nF (refer to Figure 3)		1.2		μs
Control voltage	Power Supply V <sub>DD</sub>	2.6	3.3	5.5	V
	All control pins high, V <sub>ih</sub>	1.1	3.3	5.25	V
	All control pins low, V <sub>il</sub>	-0.3		0.5	V
Control current	All control pins low, I <sub>il</sub>		0		μA
	All control pins high, I <sub>ih</sub>			7.5	μA
Current consumption, I <sub>DD</sub>	Active mode		160	200	μA

**Note:**

[1] See Fig 3 for match

[2] P0.1dB is a figure of merit.

[3] No external DC blocking capacitors required on RF pins unless DC voltage is applied on a RF pin.

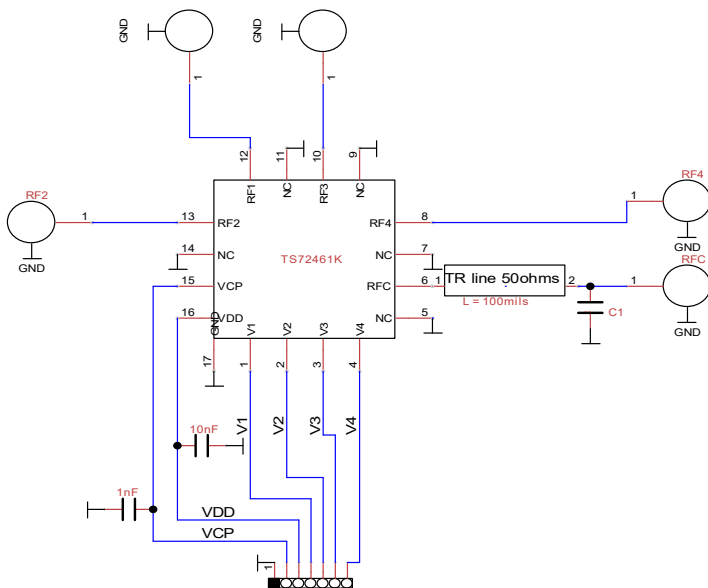
## 8.0 Switch Truth Table

**Table 5 Switch Truth Table**

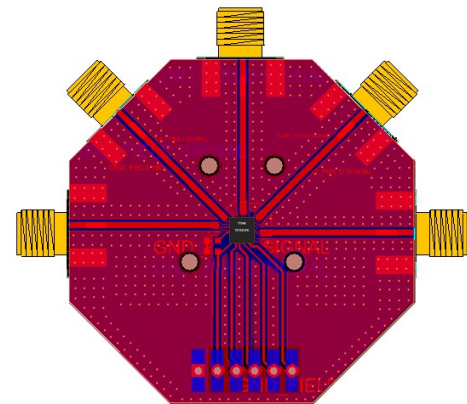
V1	V2	V3	V4	Active RF Path
0	0	0	0	All OFF State
0	0	0	1	RF4
0	0	1	0	RF3
0	0	1	1	RF3, RF4
0	1	0	0	RF2
0	1	0	1	RF2, RF4
0	1	1	0	RF2, RF3
0	1	1	1	RF2, RF3, RF4
1	0	0	0	RF1
1	0	0	1	RF1, RF4
1	0	1	0	RF1, RF3
1	0	1	1	RF1, RF3, RF4
1	1	0	0	RF1, RF2
1	1	0	1	RF1, RF2, RF4
1	1	1	0	RF1, RF2, RF3
1	1	1	1	All ON. RF1, RF2, RF3, RF4

**Attention:** VDD should be applied first before V1 to V4, otherwise may cause damage to the device.

## 9.0 Evaluation Board



**Figure 3 Evaluation Board (Tuned for 3.3-3.8GHz)**



**Figure 4 Evaluation Board Image**

**Attention:**

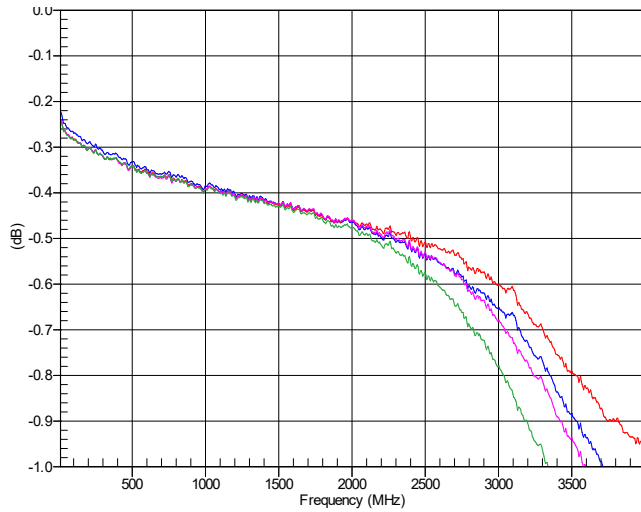
[1] 17 refers to the center pad of the device.

[2] The purpose of connection between VCP and connector N1 is to monitor VCP, do not apply external voltage to VCP.

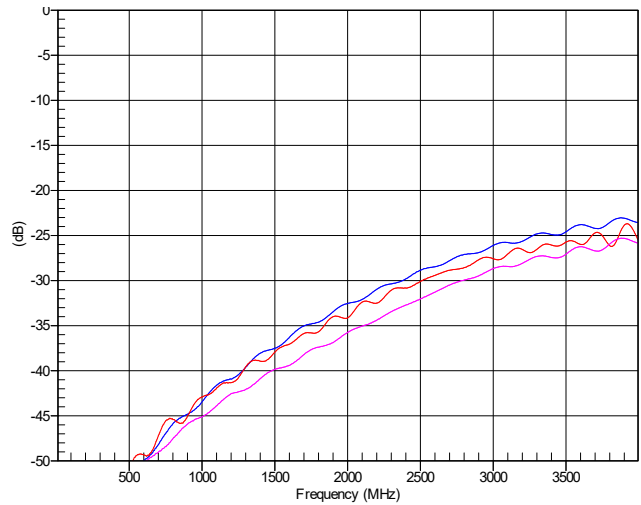
**Table 6 Recommended Evaluation Board Component Values**

Part #	Frequency Band: 3.3GHz~3.8GHz	
	Value	Manufacturer, Part#, Series
Transmission Line	50 ohms	Length 100 mils
C1	0.5pF	Passive Plus, 0603N Series

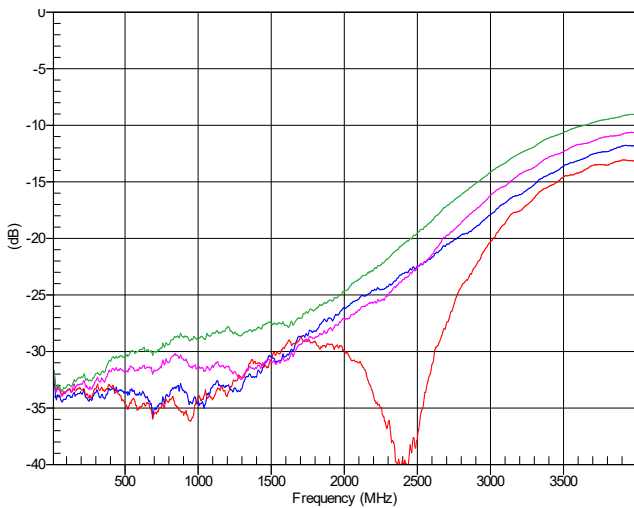
**10.0 Typical Characteristics (No Match)**



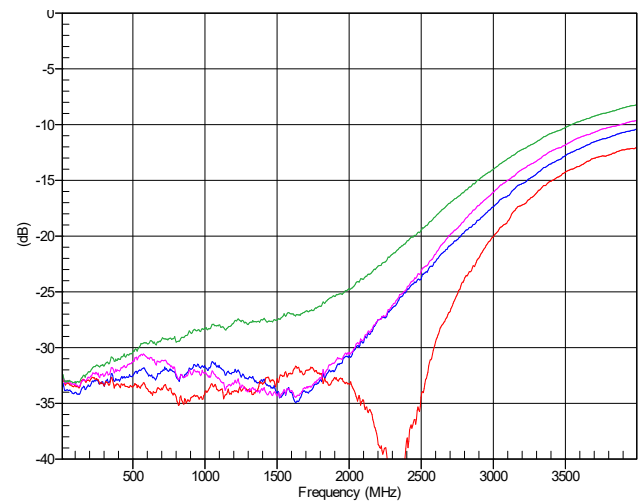
**Figure 5 RF1 to RF4 Insertion Loss**



**Figure 6 RF1 ON, RF1 Isolation to RF2 to RF4**

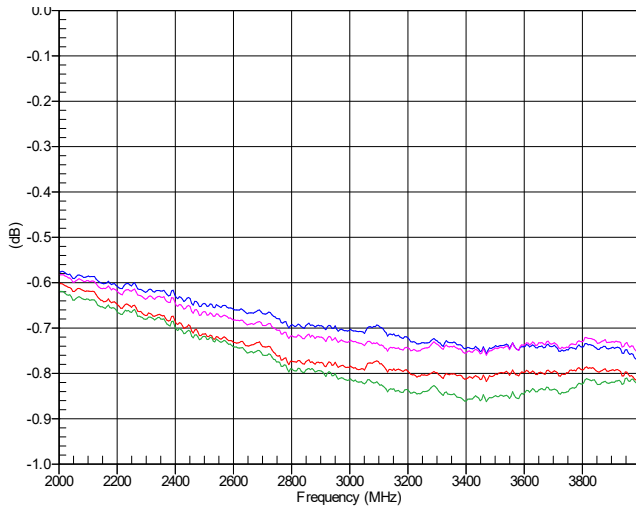


**Figure 7 RF1 to RF4 Return Loss**

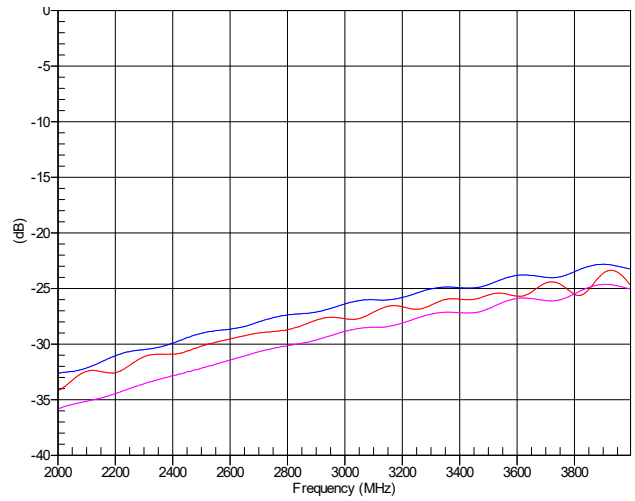


**Figure 8 ANT Return Loss**

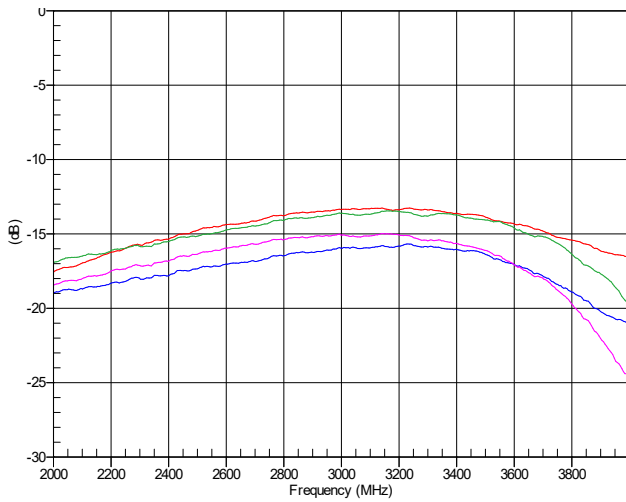
**11.0 Typical Characteristics (With Match – Tuned for 3.3-3.8GHz)**



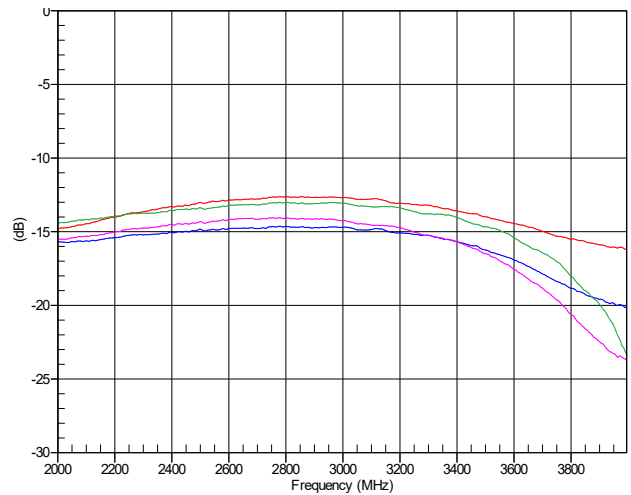
**Figure 5 RF1 to RF4 Insertion Loss**



**Figure 6 RF1 ON, RF1 Isolation to RF2 to RF4**

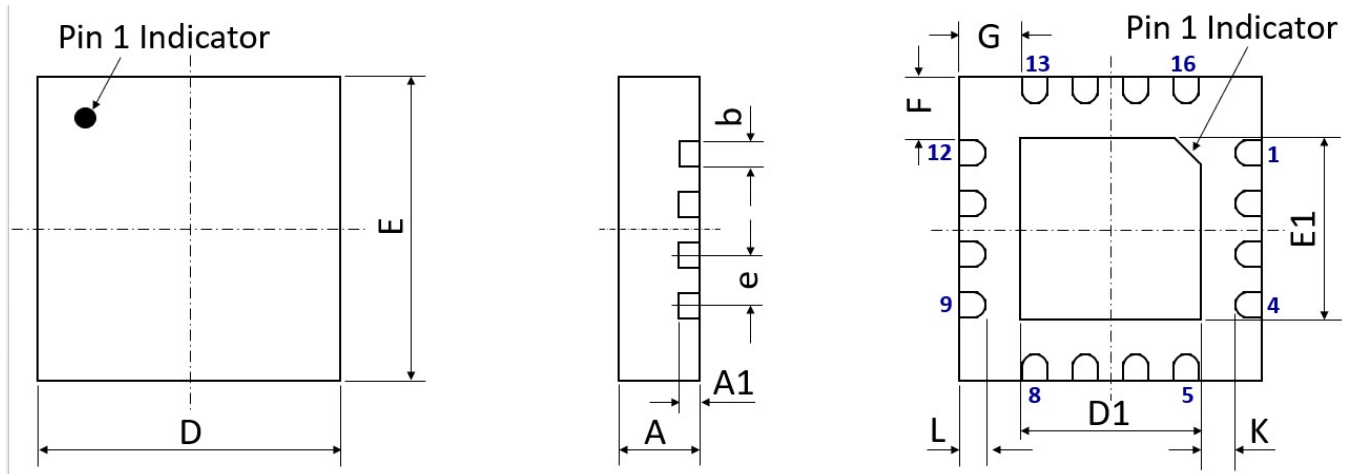


**Figure 7 RF1 to RF4 Return Loss**



**Figure 8 ANT Return Loss**

## 12.0 Device Package Information



**Figure 9 Device Package Drawing**  
 (All dimensions are in mm)

**Table 7 Device Package Dimensions**

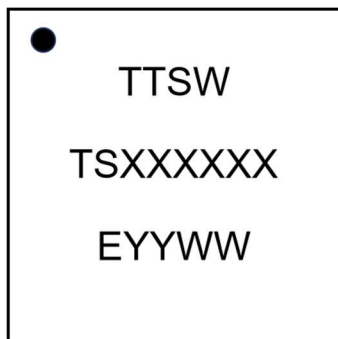
Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A	0.80	±0.05	E	3.00 BSC	±0.05
A1	0.203	±0.02	E1	1.70	±0.05
b	0.25	+0.05/-0.07	F	0.625	±0.05
D	3.00 BSC	±0.05	G	0.625	±0.05
D1	1.70	±0.05	L	0.25	±0.05
e	0.50 BSC	±0.05	K	0.40	±0.05

**Note:** Lead finish: Pure Sn without underlayer; Thickness: 7.5µm ~ 20µm (Typical 10µm ~ 12µm)

**Attention:**

Please refer to application notes [TN-001](#) and [TN-002](#) at <http://www.tagoretech.com> for PCB and soldering-related guidelines.

**Top-marking specification:**

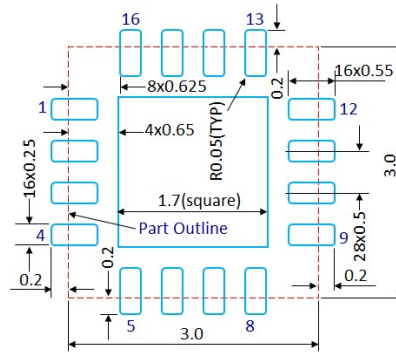


- = Pin 1 indicator
- TTSW = Tagore Technology SWitch
- TSXXXXXX = Part number (8 digits max)
- E = A fixed letter before the date code
- YY = Last two digits of assembly year
- WW = Assembly work week

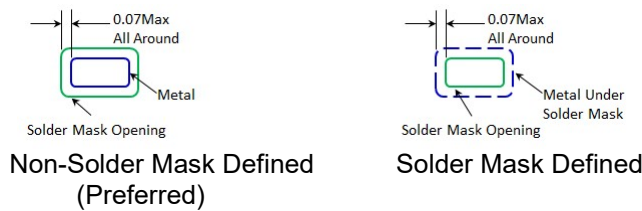
### 13.0 PCB Land Design

**Guidelines:**

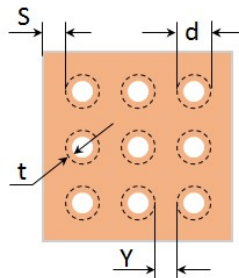
- [1] 4 layer PCB is recommended.
- [2] Via diameter is recommended to be 0.2mm to prevent solder wicking inside the vias.
- [3] Thermal vias shall only be placed on the center pad.
- [4] The maximum via number for the center pad is  $3(X) \times 3(Y) = 9$ .



**Figure 10 PCB Land Pattern**  
(Dimensions are in mm)



**Figure 11 Solder Mask Pattern**  
(Dimensions are in mm)



**Figure 12 Thermal Via Pattern**  
(Recommended Values:  $S \geq 0.15\text{mm}$ ;  $Y \geq 0.20\text{mm}$ ;  $d = 0.2\text{mm}$ ; Plating Thickness  $t = 25\mu\text{m}$  or  $50\mu\text{m}$ )

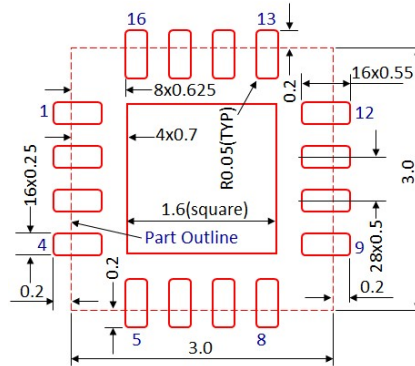


## 14.0 PCB Stencil Design

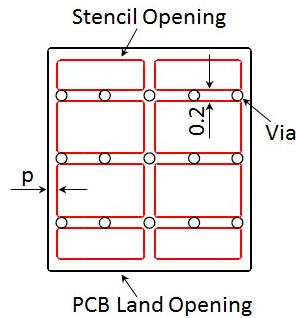
### Guidelines:

[1] Laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release.

[2] Stencil thickness is recommended to be 125 $\mu$ m.

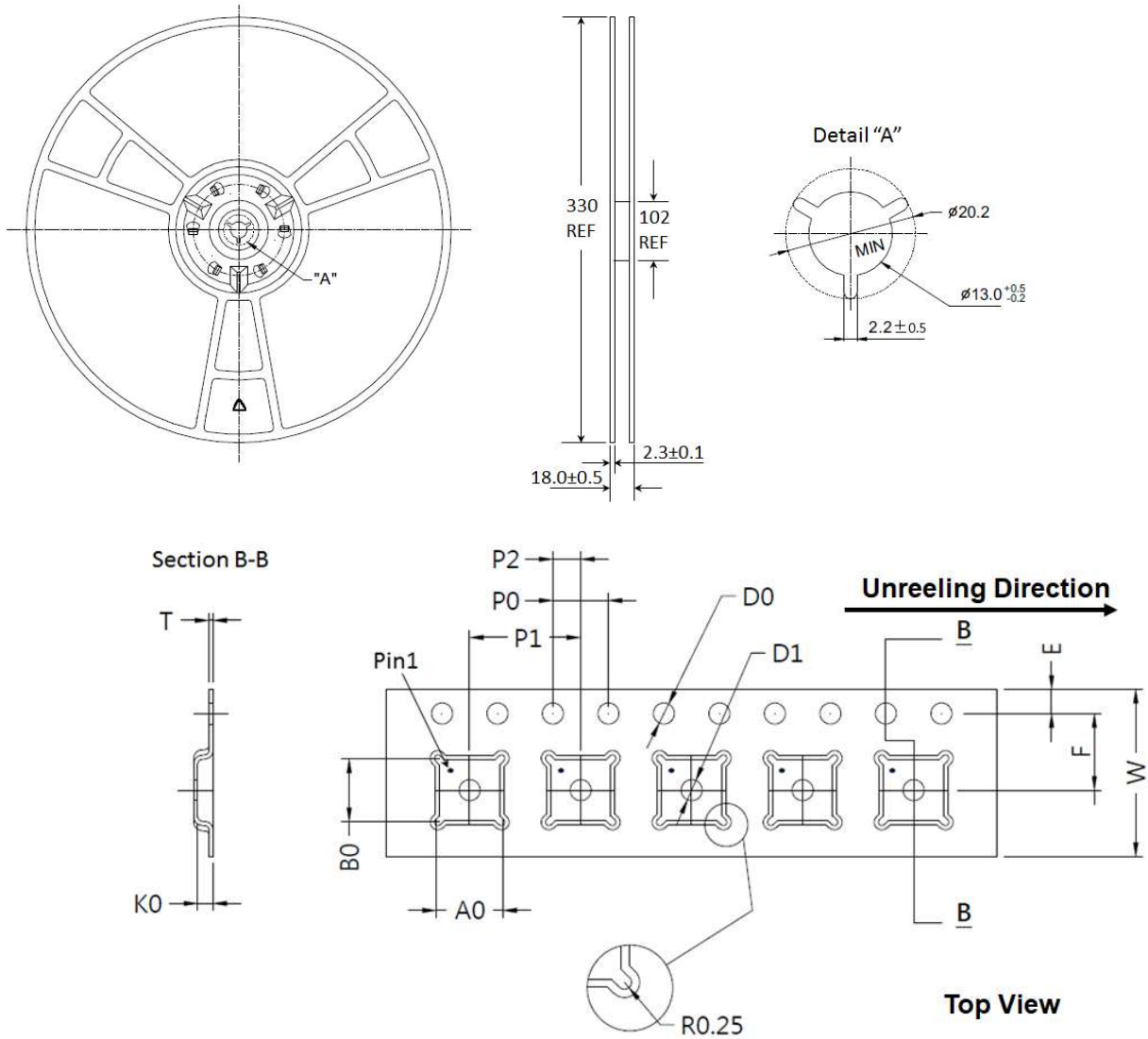


**Figure 13 Stencil Openings**  
(Dimensions are in mm)



**Figure 14 Stencil Openings Shall not Cover Via Areas If Possible**  
(Dimensions are in mm)

**15.0 Tape and Reel Information**



**Figure 15 Tape and Reel Drawing**

**Table 8 Tape and Reel Dimension**

Dimension (mm)	Value (mm)	Tolerance (mm)	Dimension (mm)	Value (mm)	Tolerance (mm)
A0	3.35	±0.10	K0	1.10	±0.10
B0	3.35	±0.10	P0	4.00	±0.10
D0	1.50	+0.10/-0.00	P1	8.00	±0.10
D1	1.50	+0.10/-0.00	P2	2.00	±0.05
E	1.75	±0.10	T	0.30	±0.05
F	5.50	±0.05	W	12.00	±0.30

**Edition Revision 2.0 - 2024-08-27**

**Published by**

TagoreTech Inc.  
601 Campus Drive, Suite C1  
Arlington Heights, IL 60004, USA

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